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PATENT FOR

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Sharad Kapur, et al.

Serial No.:

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Filed:

October 26, 1999

For:

SYSTEM AND METHOD FOR DETERMINING CAPACITANCE FOR

LARGE-SCALE INTEGRATED CIRCUITS

Group No.:

2123

Examiner:

Eduardo Garcia-Otero

Commissioner for Patents Washington, D. C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 2021, on 11 26 2002. (Date)

(Printed or/typed name of person signing the certificate

Sir:

"REQUEST FOR APPROVAL OF PROPOSED DRAWING CORRECTION"

FIGURE 2 has been modified to FIGURE 2A and FIGURE 2B has been added to provide an understanding of the subject matter as requested by the Examiner. Since this aspect of the present invention was submitted in the application as originally filed, the corrected and additional drawing do not constitute new matter. The Applicants hereby submit a proposed drawing correction for the appropriate figures in which the proposed corrections are marked in red ink. Accordingly, approval of the proposed drawing correction is respectfully requested.

In the event that the proposed drawing correction is not approved in its entirety, the undersigned will attend to the correction of these drawings in the manner specified by the Examiner.

Respectfully submitted,

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